Simulink® Design Verifier™ Release Notes

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Summary by Version

This table provides quick access to what's new in each version. For clarification, see "Using Release Notes" on page 1.

Version (Release)	New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Latest Version V1.3 (R2008b)	Yes Details	Yes Summary	Bug Reports Includes fixes	Printable Release Notes: PDF Current product documentation
V1.2 (R2008a)	Yes Details	No	Bug Reports Includes fixes	No
V1.1.1 (R2007b+)	No	No	Bug Reports Includes fixes	No
V1.1 (R2007b)	Yes Details	No	Bug Reports Includes fixes	No
V1.0 (R2007a+)	Yes Details	No	Bug Reports	No

Using Release Notes

Use release notes when upgrading to a newer version to learn about:

- New features
- Changes
- Potential impact on your existing files and practices

Review the release notes for other MathWorks™ products required for this product (for example, MATLAB® or Simulink®) for enhancements, bugs, and compatibility considerations that also might impact you.

If you are upgrading from a software version other than the most recent one, review the release notes for all interim versions, not just for the version you are installing. For example, when upgrading from V1.0 to V1.2, review the release notes for V1.1 and V1.2.

What's in the Release Notes

New Features and Changes

- New functionality
- Changes to existing functionality

Version Compatibility Considerations

When a new feature or change introduces a reported incompatibility between versions, the **Compatibility Considerations** subsection explains the impact.

Compatibility issues reported after the product is released appear under Bug Reports at the MathWorks Web site. Bug fixes can sometimes result in incompatibilities, so you should also review the fixed bugs in Bug Reports for any compatibility impact.

Fixed Bugs and Known Problems

The MathWorks offers a user-searchable Bug Reports database so you can view Bug Reports. The development team updates this database at release time and as more information becomes available. This includes provisions for any known workarounds or file replacements. Information is available for bugs existing in or fixed in Release 14SP2 or later. Information is not available for all bugs in earlier releases.

Access Bug Reports using your MathWorks Account.

Version 1.3 (R2008b) Simulink Design Verifier Software

This table summarizes what's new in V1.3 (R2008b):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	Yes Summary	Bug Reports	Printable Release Notes: PDF Current product documentation

New features and changes introduced in this version are:

Simulink Bus Signals and Bus Objects Support

Simulink® Design Verifier™ now supports Simulink buses and bus objects:

- The root Inport and Outport blocks accept bus signals.
- Nonvirtual buses are propagated through the model elements.
- The test harness model reconstructs the needed bus signals from the underlying bus elements.

Fixed-Point Data Support

Simulink Design Verifier blocks now support fixed-point parameters and inputs. These blocks include:

- Test Condition
- Test Objective
- Assumption
- Proof Objective

The `Slvd.Point` and `Sldv.Interval` constructors now accept fixed-point data.

Generating Test Harness Model with Model Reference

To use this option, select **Reference input model in generated harness** in the **Design Verifier > Results** pane of the Configuration Parameters dialog box. Simulink Design Verifier software then uses model reference to run the original model from the test harness.

Generating SystemTest TEST-File

To use this option, select **Save test harness as SystemTest TEST-File** in the **Design Verifier > Results** pane of the Configuration Parameters dialog box. The software creates a TEST-file instead of a test harness model. Using a TEST-file allows you to run the test cases in the SystemTest™ environment and configure the model coverage settings using the SystemTest software.

Improved Search Algorithms

This release includes search algorithms for the following two modes that improve the performance and the quality of the results:

- Test case generation — The combined objectives options minimizes the number of test cases by generating cases that address more than one test objective.
- Property proving — Proving that model properties are valid.

New Data File Format

When the Simulink Design Verifier software completes an analysis, it creates a data file. Now the data file supports bus input ports and includes more information about the analyzed model. For more information, see "Examining Simulink Design Verifier Data Files" in the Simulink Design Verifier documentation.

Compatibility Considerations

To convert an `sldvData` structure from the old format to the new format, use the `Sldv.DataUtils.convertToCurrentFormat` utility with the following syntax:

```
new_sldvData = Sldv.DataUtils.convertToCurrentFormat(model, old_sldvData)
```

The arguments used for this conversion comprise:

- `model` — The name of the model that was analyzed
- `old_sldvData` — The name of an `sldvData` structure created using the old (pre-R2008b) format

To convert an `sldvData` structure in the new format to the old format, use the `Sldv.DataUtils.convertToOldFormat` utility with the following syntax:

```
old_sldvData = Sldv.DataUtils.convertToOldFormat(model, new_sldvData)
```

The arguments used for this conversion comprise:

- `model` — The name of the model that was analyzed
- `new_sldvData` — The name of an `sldvData` structure created using the format that is new with R2008b

New HTML Report

The HTML report that Simulink Design Verifier software generates has been enhanced. Now, when you select **Generate report of the results** in the **Design Verifier > Report** pane of the Configuration Parameters dialog box, the report generated has several improvements:

- The report generates faster and is easier to understand.

- The report can display expected outputs.
- The software generates a report that reflect the analysis settings (for example, test case generation vs. property proving).

Blocks with No Input Ports Limitation

If a Simulink model has any blocks with no input ports, Simulink Design Verifier software cannot generate the test harness.

Version 1.2 (R2008a) Simulink Design Verifier Software

This table summarizes what's new in V1.2 (R2008a):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	No	Bug Reports	Printable Release Notes: PDF Current product documentation

New features and changes introduced in this version are

Embedded MATLAB Subset Support

This release provides support for the Embedded MATLAB™ Function block in the Simulink software and Embedded MATLAB functions in the Stateflow® software. For more information, see "Limitations of Support for the Embedded MATLAB Subset" in the *Simulink Design Verifier User's Guide*.

Enhanced Support for Stateflow Truth Tables

Previous releases support only the Stateflow Classic truth tables. However, this release introduces support for Embedded MATLAB truth tables in the Stateflow software, which includes support for the Truth Table block. See "Truth Table Functions" in the Stateflow documentation for more information.

New Simulink Design Verifier Data File Options

This release introduces new options on the **Design Verifier > Results** pane of the Configuration Parameters dialog box:

- **Include expected output values** — Simulates the model using the test case signals and includes the output values in the Simulink Design Verifier data file. See “Include expected output values” for more information.
- **Randomize data that does not affect outcome** — Assigns random values instead of zeros to input signals that have no impact on test or proof objectives. See “Randomize data that does not affect outcome” for more information.

New Test Suite Optimization Setting

In this release, the **Test suite optimization** parameter that appears on the **Design Verifier > Test Generation** pane of the Configuration Parameters dialog box includes a new setting: `Large model`. This test generation strategy is tailored to large, complex models that contain nonlinearities and many test objectives. See “Test suite optimization” for more information.

Version 1.1 (R2007b) Simulink Design Verifier Software

This table summarizes what's new in V1.1 (R2007b):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	No	Bug Reports	No

Fixed-Point Data Type Support

This release provides support for fixed-point data types. For more information, see "Limitations of Fixed-Point Support" in the *Simulink Design Verifier User's Guide*.

Version 1.0 (R2007a+) Simulink Design Verifier Software

This table summarizes what's new in V1.0 (R2007a+):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	No	Bug Reports	No

Version 1.0 of the Simulink Design Verifier software was released in a Web-downloadable form after R2007a.

Introducing the Simulink Design Verifier Software

The Simulink Design Verifier software extends the Simulink and Stateflow products with formal methods that help you confirm your models and charts behave correctly. The Simulink Design Verifier software performs a mathematically rigorous analysis of your model to identify all of its possible execution pathways. Subsequently, the software can

- **Generate Tests**

  The Simulink Design Verifier software can generate tests that satisfy your model's coverage objectives, including decision coverage, condition coverage, and modified condition/decision coverage (MC/DC). You can even customize the tests that it generates by using Simulink Design Verifier blocks that allow you to specify your own objectives and to constrain signal values. After the software completes its analysis, it produces a test harness model with a Signal Builder block that contains test signals. Simply simulate the test harness model to confirm that the test signals achieve your model's objectives.

- **Prove Properties**

  The Simulink Design Verifier software can prove that signals in your model attain particular values or ranges. Use Simulink Design Verifier blocks to specify values and ranges that you desire signals to attain, or to constrain the values of other signals. If the software disproves any of the values or ranges given the constraints you specify, it produces a test

harness model with a Signal Builder block that contains signals comprising counterexamples. Simply simulate the test harness model to confirm that the counterexamples falsify your model's properties.

The Simulink Design Verifier software documents its analysis results in an HTML report. Also, it produces a data file containing the analysis results, which you can postprocess for your own analyses and reports.

In short, the Simulink Design Verifier software gives you confidence in the behavior of your Simulink models and Stateflow charts.

Compatibility Summary for Simulink Design Verifier Software

This table summarizes new features and changes that might cause incompatibilities when you upgrade from an earlier version, or when you use files on multiple versions. Details are provided in the description of the new feature or change.

Version (Release)	New Features and Changes with Version Compatibility Impact
Latest Version V1.3 (R2008b)	See the **Compatibility Considerations** subheading for each of these new features or changes: • "New Data File Format" on page 5
V1.2 (R2008a)	None
V1.1 (R2007b)	None
V1.0 (R2007a+)	None